High-Q Copper Inductors on Standard Silicon Substrate with a Low-k BCB Dielectric Layer

Xiao Huo, Kevin J. Chen and Philip C. H. Chan

Dept. of Electrical and Electronic Engineering, Hong Kong University of Science and Technology
Clear Water Bay, Kowloon, Hong Kong

Abstract — **High-Q Cu inductors using low-k BENZOCYCLOBUTENE (BCB) dielectric as an interface layer have been fabricated on standard CMOS-grade silicon substrate. Metal ohmic loss and substrate loss, the two major factors that degrade the Q-factors of on-chip inductors, are suppressed by the employment of electroplated copper and the BCB dielectric, respectively. Quality-factor as high as 25 was obtained for a 1-nH inductor at 2 GHz. The inductor fabrication process is low-cost and low-temperature, making it suitable for post-IC process for high-performance RFIC's and MMIC's.**

I. INTRODUCTION

On-chip high-Q inductors are key elements in high-performance radio-frequency (RF) and microwave front-end integrated circuits, such as voltage controlled oscillators (VCO's), low-noise amplifiers (LNA's), filters as well as the indispensable impedance matching networks [1]-[3]. The planar spiral inductors integrated on the low-cost standard (low resistivity, CMOS-grade) silicon substrate using standard silicon technology and aluminum metal interconnects have shown poor Q-factor (around 5) due to the severe substrate loss of the standard silicon substrate at microwave frequencies and the ohmic loss of the aluminum thin-film. As a result, novel low-cost technologies need to be introduced for fabricating silicon-based high-Q inductors for the high-performance single-chip RFIC's and MMIC's. While the ohmic loss can be reduced by using high-conductivity metals such as Copper [4] or gold [5], the reduction of the substrate loss remains the major hurdle for silicon-based on-chip inductors. To overcome the substrate loss, several approaches have been implemented with improved Q-factor. Ground-shielded inductors have been devised to reduce the substrate loss and noise coupling [6], with limited improvement in Q-factor (up to 10). Suspended inductors with the inductor metal separated from the lossy silicon substrate have offered Q factors as high as 50 at 7 GHz [7]. However, the practical implementation of the suspended inductors could be hindered by the additional cost associated with the expensive processes (i.e., micromachining) and the weak mechanical strength of the hanging inductors.

Another approach to reducing the substrate loss is to insert low-loss low-k dielectric layers between the inductor metal and the lossy silicon substrate. Cu inductors using polyimide as an interface layer has been demonstrated, showing Q-factor as high as 17 at 2 GHz. [8]. However, reliability issues may arise for this technology since Cu drifts readily into polyimide [9]. Another low-k dielectric, benzocyclobutene (BCB), exhibits much slower Cu drift, providing a preferred material choice for improved reliability. High-Q inductors employing BCB dielectric has been demonstrated in a multi-chip-module (MCM) on glass substrates [10]. In this paper, we report a low-cost silicon-based on-chip inductor technology employing electroplated Cu layer and spin-on BCB interface layer. Q-factors as high as 25 were obtained for a 1-nH inductor at 2 GHz.

II. FABRICATION

The fabrication process and the cross-sectional schematic of the on-chip spiral inductors are illustrated in Fig. 1. The inductors were fabricated on a CMOS-grade p-type silicon substrate with a resistivity of 20 Ω·cm.

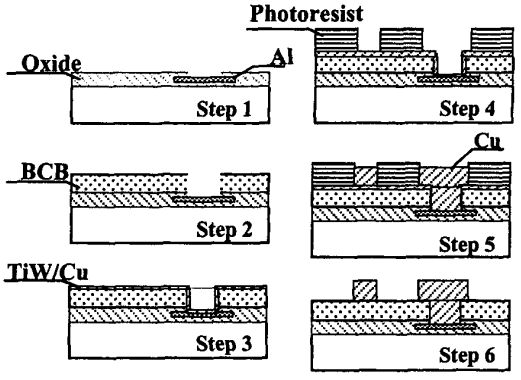

Fig.1. Process flow and cross-sectional schematic of the high-Q inductors: Step 1): oxide and metal one (aluminum) patterning; 2) BCB coating and via opening; 3) TiW/Cu seed layer sputtering; 4) Thick PR coating and patterning; 5) electroplating copper; 6) PR and TiW/Cu seed layer removal.

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Aluminium metal strips (0.5 μm) sandwiched by 0.5 μm oxide layers (both below and above) were first fabricated on the silicon substrate to simulate a CMOS wafer after the conventional Al-based IC process. The aluminium strips can provide the interconnections between the inductors and the CMOS integrated circuits on the same wafer. A photosensitive 6 μm thick BCB layer was then spin-coated (1500 rpm) and patterned. Via holes (15 μm wide) were opened on the aluminium strips for contacts with Cu. After the curing process of the BCB layer, a thin TiW (thickness 80 nm) and copper seed layer (thickness 350 nm) was sputtered on the silicon wafer. A thick photoresist layer was then coated on the wafer and the inductor pattern was defined by photolithography. The copper metallization was completed using electroplating technique. The copper thickness is decided by the photoresist thickness (controlled by the spinning speed). Finally, the photoresist and TiW/Cu seed layers were removed by chemical stripping and etching. It should be noted that the entire inductor fabrication is carried out below 250°C, which is suitable for post-IC process.

III. Results and Discussions

On-wafer S-parameters were measured using HP8510C network analyzer and microwave probes. Both one-port (single turn inductors) and two-port inductors (multiple turn inductors) were designed and measured. The pad-only characteristics were measured on the "open" pad pattern to extract the pad's parasitics. The pad's parasitics were then de-embedded from the overall inductor characteristics by subtracting the Y-parameters of the "open" pad from the Y-parameter of the overall inductor, and the characteristics of the de-embedded Cu-inductor were obtained.

Q-factors of the 1nH inductors with Cu thickness varying from 0.8 μm to 15 μm, were obtained from 0.1 to 16 GHz, as shown in Fig. 2. The BCB layer thickness was fixed at 6-μm. For all four different Cu thicknesses, the Q-factor reaches peak value around 2GHz. The inductor with 15 μm thick Cu reaches a maximum value of 25. The Q-factors show little difference beyond 10 GHz, indicating that the substrate loss becomes the dominant loss mechanism at higher frequencies.

From Fig. 2, it is clear that increasing the Cu thickness can improve the Q-factor. The main reason is the reduction of the series resistance of the inductors as a result of the increasing Cu thickness. However, the enhancement of Q-factor by increasing the physical thickness of Cu cannot be sustained indefinitely, especially at higher frequencies.

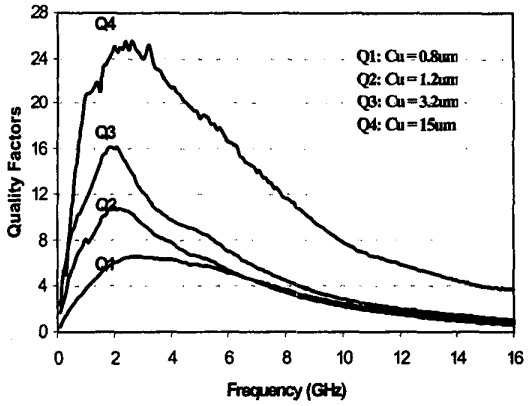

Fig.2. Comparison of Q-factors for 1-nH inductors with different copper thickness. The thickness of BCB layer is 6-μm.

This is mainly due to the fact that the series resistance will reach a "saturation" value as a result of the saturating effective thickness of the inductor metal (Cu). The effective thickness, t_{eff}, is related to the physical thickness of the inductor metal, t, by [11]

$$t_{eff} = \delta \cdot (1 - e^{-t/\delta}) \qquad (1)$$

where $\delta = \sqrt{\frac{\rho}{\pi \mu f}}$ is the skin depth of Cu that can be determined by ρ (Cu resistivity), μ (Cu permeability) and f (frequency).

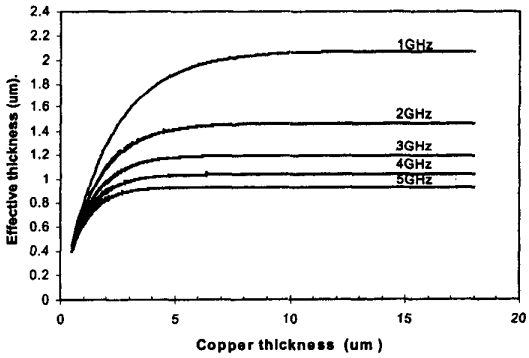

Fig.3 Effective copper thickness for different frequency

The saturation of the effective Cu thickness for different frequencies is illustrated in Fig. 3. Between 1GHz and 2GHz, the increase in physical thickness of Cu up to 10 μm substantially increases the effective thickness, resulting in reduced series resistance and enhanced Q-factor. Any

increase in the physical thickness of Cu beyond 10 μm will have minimal effect on the enhancement of the Q-factor.

The use of low-k BCB dielectric reduces the coupling between the inductor and the lossy silicon substrate, and therefore enhances the Q-factor. As the BCB layer thickness increases, the frequency at which the substrate lose becomes significant also increases, resulting in higher Q-factor at higher frequency. Fig. 4 shows the Q-factor of the 1nH inductors with 6- and 12-um BCB. The copper thickness for these inductors is fixed at 6um. Substrate effect is effective suppressed for the inductor with thick BCB. The improvement becomes more significant for frequencies higher than 2GHz.

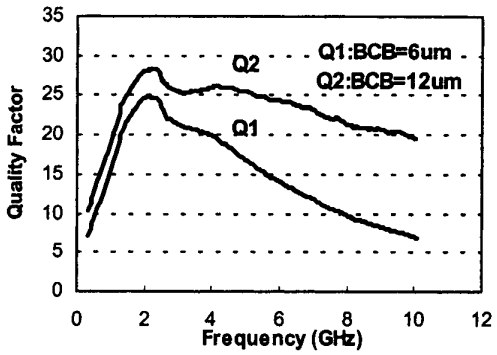

Fig.4. Comparison of Q-factors for 1-nH inductors with different BCB thickness. The thickness of copper layer is 6um.

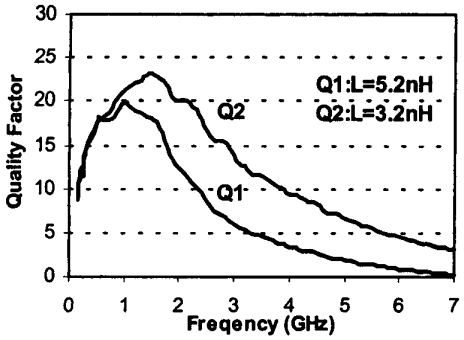

Fig. 5 Quality factors for inductors of different inductance values with the same outer dimension on the same wafer. (Cu=6um, BCB=6um)

Since the inductor-substrate coupling is proportional to the planar area of the inductor, larger inductors will have stronger coupling effect due to its larger number of turns and periphery. The Q-factor of two different inductors (3.2 and 5.2 nH, respectively) is plotted in Fig. 5. The copper and BCB thickness are 6um and 9um, respectively. The 3.2nH inductor has a higher quality factor compared with the 5.2nH one, because of the smaller number of turns and the smaller physical size.

An equivalent circuit, shown in Fig. 6(a), was used to model the high-Q on-chip inductors. Ls, Cs, and Rs account for the inductance, the coupling capacitance between spiral lines, and the series resistance of the inductor, respectively. Rs is frequency-dependent, as a result of the frequency-dependent skin depth. Cox accounts for the coupling capacitance between the metal (Cu) and the lossy silicon substrate. Csi and Rsi account for the substrate capacitance and resistance.

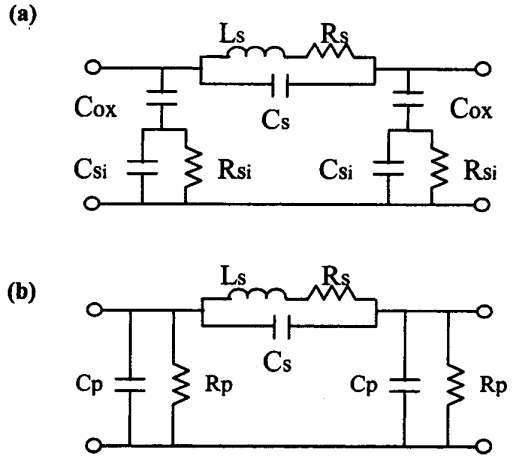

Fig.6. Two-port lumped equivalent circuit model (a) and the corresponding simplified model (b) of the inductors.

The equivalent circuit model in Fig. 6(a) can be simplified to Fig. 6(b) by combining the impedance of Cox, Csi, and Rsi, as given by [12],

$$R_P = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si}(C_{ox}+C_{Si})^2}{C_{ox}^2} \tag{3}$$

$$C_P = C_{ox} \cdot \frac{1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2}{1+\omega^2(C_{ox}+C_{Si})^2 R_{Si}^2} \tag{4}$$

Two-port model extraction was carried out to obtain the component values in the equivalent circuit. Comparison between the measured and simulated results is shown in Fig.7 (a) and (b) for a 5.2 nH inductor with 6 μm copper and 6 μm BCB. Excellent agreement is achieved for S-parameters (S_{11} and S_{12}), in both magnitude and phase.

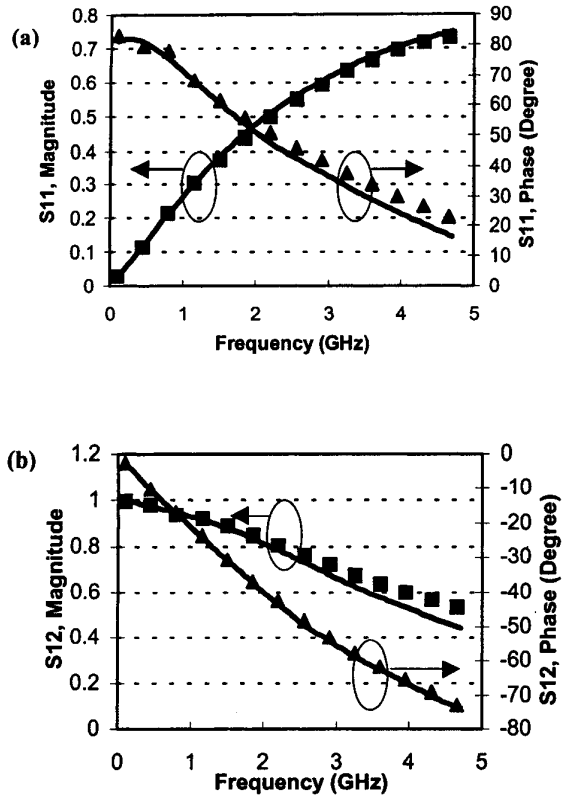

Fig.7. Model Extraction results of the two-port S-parameters for the 5.2 nH inductor. (a) (S11) magnitude and phase. (b) (S12) magnitude and phase. Square denotes the magnitude of measured results, triangle denotes the phase of measured results and solid line denotes simulated result.

IV. CONCLUSION

High-Q inductors employing electroplated Cu and a BCB dielectric interface layer have been demonstrated on standard silicon substrates. By using simple electroplating technique, copper inductors with different thickness were built. Low-resistivity Cu reduces ohmic loss and the thick BCB layer reduces the substrate loss. Inductors ranging from 1 nH to 5.2 nH exhibit high Q-factors that have peak values above 20. This process can be readily used as a post-IC process for single-chip implementation of RFIC's and MMIC's.

ACKNOWLEDGEMENT

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REFERENCES

[1] T. H. Lee, *The design of CMOS Radio-Frequency Integrated Circuits.* Cambridge,U.K.: Cambridge Univ. Press 1998.

[2] D. K .Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier." *IEEE Journal of Solid-State Circuits*, vol.32, no.5, pp.745-759, May 1997.

[3] M. D. M. Hershenson, A. Hajimiri, S. S. Mohan, S. P. Boyd and T. H. Lee. "Design and optimization of LC oscillators." *1999 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers* pp.65-69.

[4] H. Jiang, Yeh J-LA, Y. Wang and N. Tien. "Electromagnetically shielded high-Q CMOS-compatible copper inductors. " *2000 IEEE Int. Solid-State Circuits Conference. Digest of Technical Papers,* pp.330-331.

[5] K. Kamogawa, K. Nishikawa, I. Toyoda, T. Tokumitsu and M. Tanaka, "A novel high-Q and wide-frequency-range inductor using Si 3-D MMIC technology. " *IEEE Microwave & Guided Wave Letters,* vol.9, no.1, pp.16-18, Jan. 1999.

[6] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs. " *IEEE Journal of Solid-State Circuits,* vol.33, no.5, pp.743-752, May 1998,.

[7] Jun-Bo Yoon, Chui-Hi Han, Euisik Yoon and Choong-Ki Kim. "Monolithic high-Q overhang inductors fabricated on silicon and glass substrates. " *1999 International Electron Devices Meeting. Technical Digest,* pp.753-756.

[8] J. Rogers, T. Liang, T. Smy, N. Tait and G. Tarr, "A high Q on-chip Cu inductor post process for Si integrated circuits. " *Proceedings of the IEEE 1999 International Interconnect Technology Conference,* pp.239-241.

[9] A.L.S. Loke, J. T. Wetzel, Changsup Ryu, Won-Jun Lee and S. S. Wong. " Copper drift in low-k polymer dielectrics for ULSI metallization," *1998 Symposium on VLSI Technology Digest of Technical Papers,* pp.26-27.

[10] P. Pieters, K. Vaesen, W. Diels, G. Carchon, S. Brebels, W. De Raedt, E. Beyne and R. P. Mertens. " High-Q integrated spiral inductors for high performance wireless front-end systems. " *2000 IEEE Radio and Wireless Conference* pp.251-254.

[11] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon. " *IEEE Transactions on Electron Devices,* vol.47, no.3, pp.560-568, March 2000.

[12] C. P. Yue and S. S. Wong. "On-Chip spiral iductors with patterned ground shields for Si-Based RF IC's. " *IEEE Journal of Solid-State Circuits,* vol.33, pp.743-752, May 1998.